REMARKS

Claims 41-43 and 48-52 are pending in the application. Claims 48-52 are withdrawn from consideration as being directed to a non-elected species.

The Office Action summary section of the present Action sets forth claims 41-43 as pending in the application. Applicant notes however, that claims 48-52 remain pending in the application and have the status of being withdrawn from consideration as directed to a non-elected species. In applicant's response filed May 4, 2006, applicant acknowledged the Examiner's withdrawal from consideration of claims 48-52 and noted that the Examiner failed to set forth reasons such claims were held distinct as required in the MPEP (see MPEP § 809.02, 814, 816 and 817). However, the reasons for the holding of distinctness have not been presented in the present Action. The Action is therefore incomplete and the holding of finality is therefore premature. Applicant therefore requests withdrawal of the finality of the present Action and again requests that the Examiner set forth reasons for finding distinctness between species. Applicant additionally requests formal notification of withdrawal of the finality of the office action to allow a request for refund of RCE fees to be filed.

Claims 41-43 stand rejected under 35 U.S.C. § 112, first paragraph, based on lack of enablement. Claims 41-43 stand additionally rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Examiner bases the § 112 rejections upon a contention that the specification fails to teach a 5 Å thick gate oxide layer, and nitriding only the upper half of such layer. Applicant directs attention to the specification at page 4, lines 13-20 which specifically indicates gate oxide layer 14 which can comprise silicon dioxide and can have a thickness of from about 5Å to about

60Å. The subsequent paragraph beginning at page 4, line 21 and continuing through page 5, line 7, indicates that in particular embodiments the 5-60Å layer 14 contains nitrogen entirely in the upper half of such layer, an upper third of such layer, an upper fourth of such layer or an upper fifth of such layer. The specification goes on to disclose methodology for achieving such layer. Accordingly, the claim 1 recited silicon dioxide gate oxide layer having a total thickness of about 5 Å and having a nitrogen enriched region which is only in an upper half is fully disclosed and enabled by applicant's specification. Applicant therefore respectfully requests withdrawal of the rejection under § 112, first paragraph, of claims 41-43 in the Examiner's next action.

Claims 41-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma (U.S. Patent No. 5,960,302). The Examiner is reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Each of these three factors must be shown in order to establish a *prima facie* case of obviousness, the burden of which is upon the Office. Claims 41-43 are allowable over Ma for at least the reason that Ma fails to disclose or suggest each and every element in any of the claims, fails to provide motivation for modification, and fails to provide a basis for a reasonable expectation of success.

Independent claim 41 recites a transistor structure having a gate oxide layer on a semiconductive substrate where the gate oxide layer has a total thickness of 5Å. As recited in claim 41, the gate oxide layer comprises silicon dioxide and has a nitrogen enriched region which is only in an upper half of the gate oxide layer. A conductive layer is

on the gate oxide layer. The Examiner indicates at page 3-4 of the present Action that Ma discloses a gate oxide layer interpreted to be inclusive of layers 1311 and 115, and acknowledges that the minimum thickness taught by Ma would be 10Å for this layer. Accordingly, Ma fails to disclose or suggest the claim 41 recited gate oxide layer having a total thickness of 5Å. The Examiner contends however that "such a variation of thickness would have been obvious to one of ordinary skill in the art" because the Ma disclosure teaches that the total thickness of "composite gate dielectric 19 and the relative thicknesses of the dielectric sublayers may be adjusted by varying the oxidation time, temperature and gas partial pressures for individual components 1311, 115 and 17" (relying upon Ma at col. 2, ll. 14-20).

Applicant notes that the claim 41 recited gate oxide layer having a total thickness of about 5Å has a thickness which is half the minimum thickness of combined layers 1311 and 115 of Ma, which is interpreted by the Examiner as being a gate oxide layer. Accordingly, the thickness of the claim 41 recited layer differs significantly from the composite layer thickness disclosed by Ma. Further, the Ma disclosure of adjusting thicknesses of dielectric sublayers 1311, 115 and 17, when considered in context of the remaining disclosure, teaches methodology for achieving layer thickness within the disclosed range of thicknesses. Accordingly, the Ma disclosure does not disclose or suggest methodology for achieving the claim 41 recited gate oxide layer having a total thickness of 5Å with a nitrogen-enriched region only in an upper half of the gate oxide layer. In other words, Ma does not enable the thickness for which the Examiner indicates reliance upon such reference.

Applicant additionally notes that layers 1131 and 115 disclosed by Ma are separated from the disclosed substrate 11 by an additional dielectric layer 17. Accordingly, the composite layers 1311 and 115 of Ma, interpreted by the Examiner to be a gate oxide layer does not suggest the claim 41 recited gate oxide layer having a total thickness of 5Å where the gate oxide layer is on a semiconductive substrate. Ma specifically teaches a composite dielectric layer having sublayers 1311, 115 and 17 which has a minimum thickness of 15Å. Accordingly, such does not disclose or suggest the recited gate oxide layer having a total thickness of about 5Å.

In addition to the above, the Ma disclosure fails to provide motivation for modification of the disclosed minimum 15Å dielectric thickness. With respect to the motivation element to support a *prima facie* obviousness rejection, the Federal Circuit has indicated that the factual inquiry to combine or modify must be based on objective evidence of record, see *In re* Lee 61 USPQ 2d 1430 (Fed. Cir. 2002); and *In re* Fritch 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992). The Court has indicated that the factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority and stated that deficiencies of cited references cannot be remedied by general conclusions about what is basic knowledge or common sense but must be based on evidence. In the instant case, the record is entirely devoid of any evidence to support motivation to modify the teachings of Ma to produce the claim 41 recited gate oxide layer having a total thickness of 5Å which is in fact only one third of the minimum thickness of the composite dielectric layers of Ma (1311, 115 and 17 at minimum 5Å each).

In addition to failing to suggest each and every claim limitation and failing to provide motivation, the Ma disclosure does not provide a basis for a reasonable expectation of

success. As indicated above, the Ma disclosure does not enable a gate oxide layer having a total thickness of about 5Å where only an upper half of the gate oxide layer is a nitrogen-enriched region. Nor does the Ma disclosure provide a basis for a reasonable expectation that the recited gate oxide layer of about 5Å would be suitable for its intended purpose in the recited transistor structure.

The above arguments with respect to the § 103 rejection of claim 41 were presented in applicant's response filed May 4, 2006. At page 5 of the present Action the Examiner responds to such arguments indicating such are not persuasive. The Examiner again contends that no support was found in applicant's specification for a gate oxide of 5 Å. Such contention was addressed above and such gate oxide layer is fully supported by applicant's specification. The Examiner further indicates that without some unexpected results, the range of thickness is considered obvious. In this regard, the applicant requests reconsideration.

Referring to Ma at column 1, lines 10-25, applicant notes that the goal of Ma is to decrease the gate dielectric to allow decreased integrated circuit geometries. The achieved thickness disclosed by Ma is 15 Å. Accordingly, the 5 Å thick achieved by applicant's invention is unexpected as compared to Ma. Further, the ability to produce a gate oxide layer of 5 Å thick having nitride in only the upper half, is an additional unexpected result. Accordingly, a *prima facie* case of obviousness has yet to be established regarding claim 41.

Dependent claims 42-43 are allowable over Ma for at least the reason that they depend from allowable base claim 41.

For the reasons discussed above, claims 41-43 are allowable. Accordingly, applicant respectfully requests formal allowance of such claims in the Examiner's next action.

Respectfully submitted,

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